CMOS Realization of OTA as an Application in Low Power Amplifier for Enhancing the Performance and Stability using 65 Nm Technology

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Abstract: *This paper presents CMOS realization of Operational Transconductance Amplifier (OTA) as an application in low power amplifier. The proposed OTA based presents a feed forward cascode structure and differential current reduction techniques (DCRT).OTA based low power amplifier configuration employs ten MOS transistors for improving the performance and stability with a low supply voltage ± 0.70 V with high Linearity and large transconductance of 61.8 µA / V - 96.8 µA / V at ± 0.50 V bias voltages. Simulation enhancing performance parameters are higher gain, wider bandwidth, faster speed of operation and also having higher dynamic range, high linearity and stability. CMOS transistor sizing with realization of folded cascode Operational Transconductance Amplifier employs two NMOS cascode and PMOS cascode. Cascode Operational Transconductance Amplifier using positive feedback with feed forward technique and frequency dependent current mirrors. The designing of the high performance analog integrated circuits in low power amplifier application with reduced channel length, smaller and reduced power supply voltage. The proposed configuration is most suitable for implementing in Analog Signal Processing & Signal Generation Circuits. The performance of the proposed low power amplifier has been verified through SPICE simulation with TSMC CMOS 65 nm process technology.*

Keywords: *Operational Transconductance Amplifier (OTA), Low Power Amplifier, CMOS Technology, Differential Inputs Differential Outputs (DIDO), Differential Current Reduction Techniques (DCRT)*

I. Introduction:

Due to recent development in VLSI Technology and in the field of microelectronics the size of the transistor decreases and power supply also decreases. An Operational transconductance amplifiers (OTAs) have play very important role in the circuit realization due to its various advantageous features such as electronic tunability of transconductance gain, larger bandwidth, high slew rate, low power consumption, small chip size and low power supply voltage. OTA does not need any resistance. Therefore it is suitable for integrated circuit implementation. OTA-C structures are highly suitable for realizing electronically tunable continuous time filters in various technologies namely BJT, CMOS and BiCMOS. An operational transconductance amplifier has been widely investigated for realizing voltage mode as well as current mode active filters and oscillators. This OTA based low power amplifier yields high impedance at the input stage and for being utilized along with the inverting input. The transconductance of the proposed low power amplifier is normally controlled by the input bias current of the OTA. Input bias current is directly proportional to the gain of the low power amplifier. OTAs have been used universally in the different areas of analog integrated circuits like active filters design, interface circuits, data converters , oscillators , Instrumentation amplifier which are having higher gain, wider bandwidth, faster speed of operation and also having higher dynamic range , high linearity and stability are the parameters required for improving the performance of the low power amplifier. CMOS realization of OTA has higher scope for realizing low power amplifier with short channel length processes compensating to the advantages to contradictory claims and it becomes more complicated due to limited intrinsic gains of the low

power amplifier. Generally OTAs employed the structures of folded cascade or cascade for presenting high gain with high linearity and stability. While using the cascade structure decreases the slew rate and also power supply voltage.

To overcome this some multistage strategies have been used for enhancing gain, input – output noise , phase margin , slew rate and reduced power consumption and also reduced supply voltage up to desired range.

II. Description of the Proposed Active Building Blocks OTA for Low Power Amplifier

An Operational Transconductance Amplifier is a voltage controlled current source (VCCS) characterized by ideally infinite impedance at the input and output terminals.

The symbolical representation of OTA is shown in the figure 1(a) Figure 1 (b) represents Equivalent Circuit of OTA respectively.

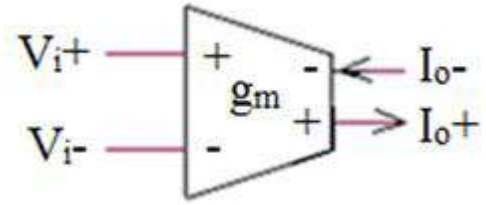

Figure 1(a) Symbolic Notation of an OTA

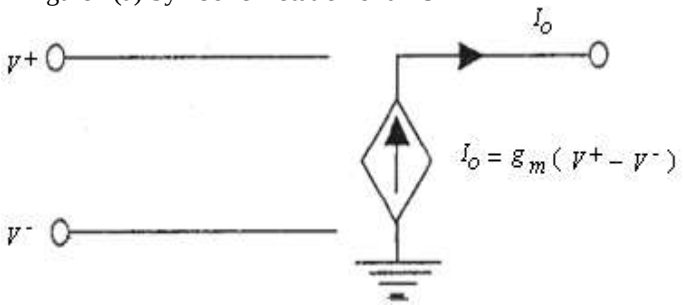

Figure 1(b) Equivalent circuit Of an OTA

Ideal Operational Transconductance Amplifier output current shows linearity with differential input voltage which is described by equation (1) :

$$I_0 = (V^+ - V^-)\, g_m \qquad (1)$$

The gain of an Ideal Operational Transconductance Amplifier is presented by equation (2).

$$\text{Gain} = \frac{V_o}{V^+ - V^-} \qquad (2)$$

$$V_{id} = (V^+ - V^-)$$

Whereas V^+ is the non-inverting input voltage, inverting input voltage is V^- and g_m is the transconductance of amplifier.

Therefore the output voltage for amplifier is given as product of its load resistance and its output current.

III. Literature Review

It has moderate impedance which is low because of Miller impact yields low linearity from a perfect OTA. 11 GHz UGBW Op amp with feedback compensation technique [1], A 1.2V pseudo differential OTA with common mode feed forward in 65nm CMOS [2], A novel operational transconductance amplifier with high Gm

using improved differential current redistribution technique (DCRT)[3], Feed forward regulated cascade OTA for Gigahertz Applications[4], Three-stage CMOS OTA for large capacitive loads with efficient frequency compensation

scheme[5], Design of Analog CMOS Integrated Circuit[6], A novel CMOS OTA based on body-driven MOSFETs and its applications in OTA-C filters[7], CMOS transconductance amplifiers, architectures and active filters: a tutorial[8], Active filter design using operational transconductance amplifiers[9],A high-swing, high impedance MOS cascode circuit[10], CMOS Circuit Design, Layout, and Simulation[11], Operational Transconductance Amplifiers for Gigahertz Applications[12], A 1-V 50- MHz pseudo differential OTA with compensation of the mobility reduction [13], An ultra-

IV. Proposed CMOS OTAs Based Configurations

a) OTAs Based Basic Differential Input Single Output Configuration

We present CMOS OTAs based basic differential input single output using feed forward cascode techniques for realizing low power amplifier. The realizing parameters have been investigated are reducing low power supply, low power consumption. The proposed configuration with low supply voltage is presented challenging task in the low-voltage ultra-low-power CMOS miller OTA with rail-to-rail input/output swing[14]. CMOS Realization of VDVTA and OTA Based fully Electronically Tunable First order all pass filter[15],OTA based Third order Quadrature Oscillator[16]. realizing of modern analog circuit.

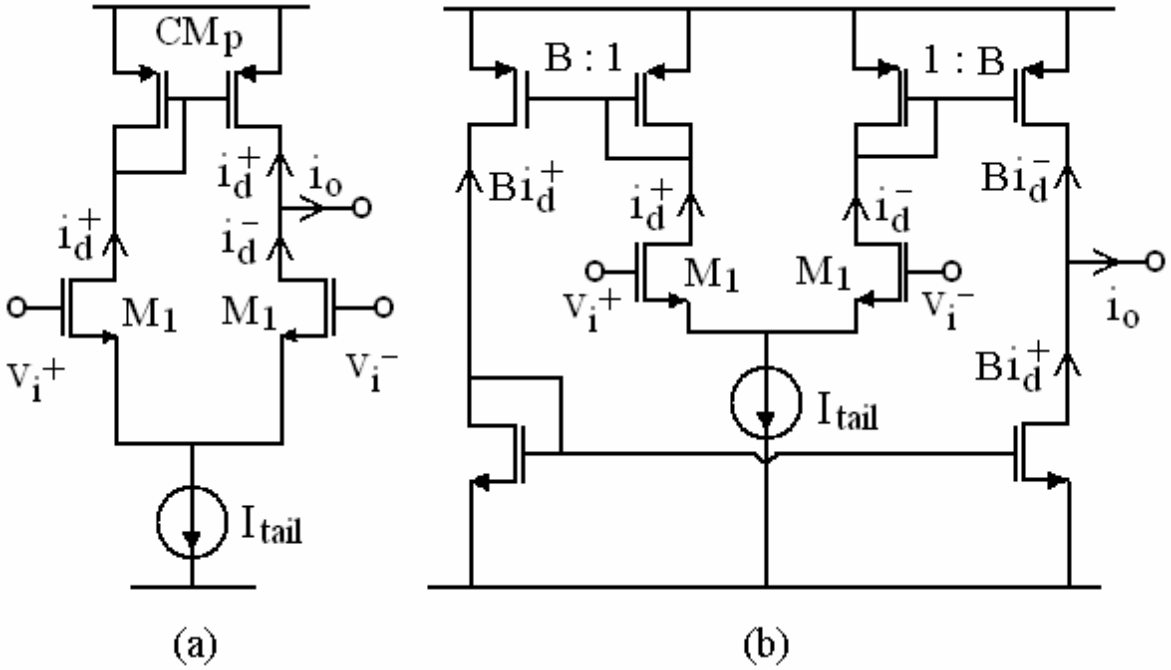

Figure 2(a).CMOS OTAs Based Differential Input Single-Output and Figure 2(b) Balanced OTA.

The Figure 2(a) present current mirror employs the implementation of CMOS OTA with the differential-input single-output structure. The balance differential OTA is shown in Figure 2(b) consist two PMOS having current mirrors can be organized in a way having size proportion of B among their controlled MOS transistor with reference transistor. The current mirror NMOS is leading in a transconductance which is large as B times of the previous ones.

These configurations present the differential-pair input stage with source-coupled. The resulting signal paths after the CMp exchanges all present left currents for differential OTAs with the differential-input single-output technique is differential input stages yields two current mirrors that plays important role id+ right current for

combining with all its right currents vi+ and vi- are differential input voltages and M1 represents the transconductance(gm) in each MOS transistor for differential pair.

b) CMOS OTA Based Cascode with Positive Feedback Configuration

The CMOS OTA based cascode configuration present an active positive feedback with feed forward technique. The realization of CMOS widely used for low power supply voltage applications in the analog circuits but has major drawback such as low gain, low slew rate and low bandwidth. The CMOS operational transconductance (OTA) based configuration have been described with excellent transconductance and linearity performance.

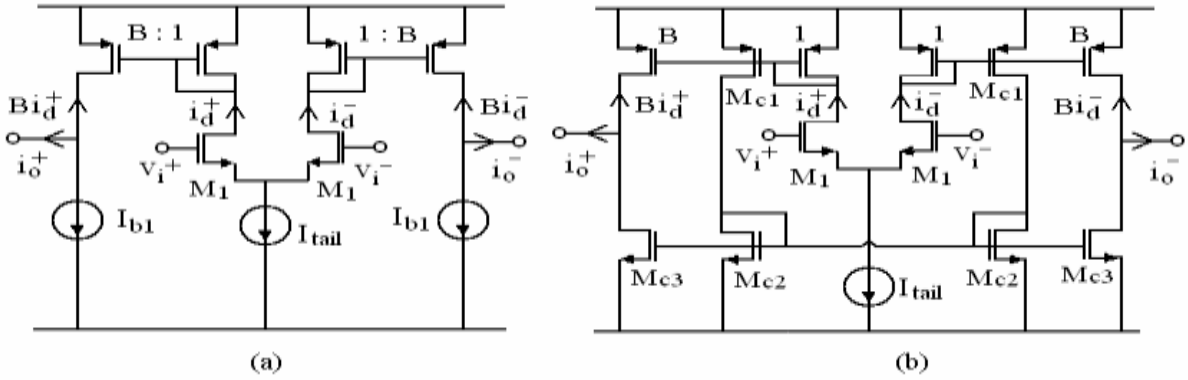

Figure 3(a) Proposed Differential Input Output CMOS OTAs and Figure 3(b) Proposed Cascode OTA using Positive Feedback with Feed Forward Technique

The DC tail currents I tail can be reported for the above transconductance tuning. Comparing to the in Figure. 3(a) and Figure 3(b) have been presented the basic positive feedback with feed forward technique containing all MC1, MC2 and MC3 to improve its normal mode. Thus sizes of MC1, MC2, and MC 3 should be appropriately chosen to present transconductance gain in common-mode of Bgm,M1, for upgrading cancellation in common-mode with the B-size for outputs PMOS transistors which have a common-mode transconductance gain of -Bgm,M1. This technique overcomes of the problems of low gain, low bandwidth, stability and level of integration. This type configuration raises problem of decrease the low output impedance and increase power supply voltage.

c) Proposed OTA Based Cascode Feed Forward Technique with Negative Feedback Configuration

The proposed CMOS OTAs based cascode feed forward technique is widely used realizing low power amplifier configuration employs ten MOS transistors with negative feedback is shown in figure 4. This OTA based cascode feed forward technique with negative feedback configuration comprises of two PMOS cascode and two NMOS cascode where PMOS and NMOS cascode have the same arrangement while their DC current are controlled with the two DC current sources at the base.

The CMOS configuration of this OTA amplifies its DC bias current and makes its output symmetric. The proposed method used negative feed forward method in place of negative feedback conventionally is presented. In this proposed circuit, four regulated cascodes are used. The two PMOS cascodes used are namely PMOS-1/PMOS-4 and PMOS-3/ PMOS-2 and two NMOS cascodes namely NMOS-2/NMOS-3 and NMOS-1/NMOS-4. The addition two MOS transistors in the cascode arrangement with negative feedback enhance stability, unity gain bandwidth, phase margin, linearity, common mode rejection ratio, input output noise and reduced the power supply voltage and power consumption of the CMOS OTAs based low power amplifier. It presents good frequency and phase response, high linearity, large bandwidth, large common mode rejection ratio and high stability.

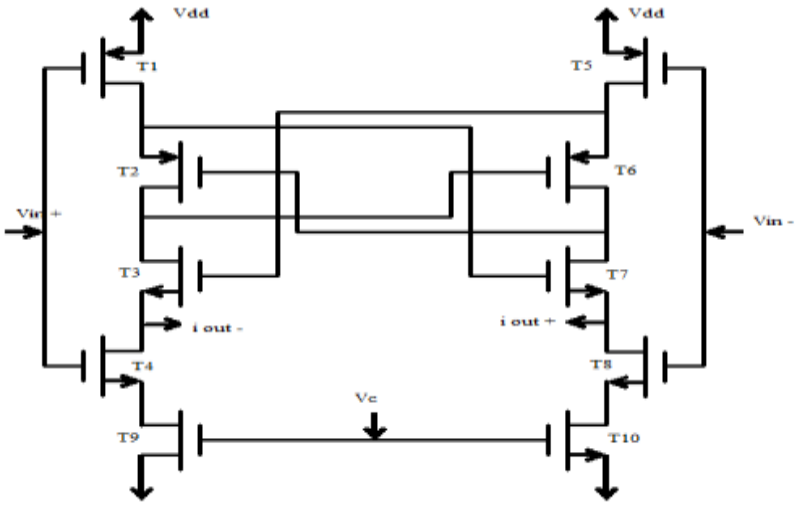

Figure 4. Proposed OTA Based Cascode Feed Forward Technique With Negative Feedback Configuration

The transconductance g_m of MOS transistor is characterized by the equation (2.1) in the weak inversion

$$g_m = \frac{IDS}{2V_T} \quad (2.1)$$

The transconductance g_m of MOS transistor is characterized by the equation (2.2) in the strong inversion

$$\sqrt{2\mu Cox\left(\frac{W}{L}\right) Ids} \quad (2.2)$$

The total gain (A) of the low power amplifier is presented by the equation (2.3)

$$A = Av_1\, Av_2 \quad (2.3)$$

The voltage gain (Av_1 & Av_2) of low power amplifier is characterized by the equations (2.4) and (2.5)

$$Av_1 = \frac{g_{m8}}{g_{m2}} = \frac{g_{m7}}{g_{m6}} \quad (2.4)$$

$$Av_2 = \frac{z_0}{2}(g_{m1} + g_{m3}) \quad (2.5)$$

The gain Av (dB) for an ideal low power amplifier is described by the equation (2.6)

$$Av(dB) = 20\log_{10}\left(\frac{V_0^+ - V_0^-}{V_i^+ - V_i^-}\right) \quad (2.6)$$

folded cascode with negative feedback is reported by the equation (2.8)

$$A_v = \frac{g_{m9}g_{m6}g_{m4}}{I_B^2(g_{m4}\lambda_n^2 + g_{m6}\lambda_p^2)} \quad (2.8)$$

The gain band width (GBW) of the low noise amplifier is characterized by the equation (2.9)

Total harmonic distortion (THD) of a low power amplifier is presented by the equation (2.7)

$$THD = 10\log\left(\frac{V_{h2}^2 + V_{h3}^3 + V_{h4}^4}{V_f^2}\right) \quad (2.7)$$

Whereas V_f is the amplitude of fundamental and V_{hi} is the amplitude of i^{th} harmonics component.The name folded cascode configuration comes from folding down N channel cascode active loads of a differential pair and changing N channel MOS to P channel. The modified gain of the proposed low power configuration employing

$$\text{Gain Band Width (GBW)} = \frac{g_{m9} I_D}{I_D C_l} \qquad (2.9)$$

Whereas λ_n and λ_p are the channel length modulation for N channel and P channel.
The gain of the low power amplifier is presented by the equation (3.0) with the folded cascode circuits which employs ten MOS transistors

$$A_v = \frac{g_{m9} g_{m6}}{I_D^2(\lambda_n^2+\lambda_p^2)} \qquad (3.0)$$

The Figure of Merit (FOM) of the proposed CMOS OTA based low power Amplifier can be described by the equation (3.1)

$$\text{Figure of Merit (FOM} = \frac{GWB.C_L}{I_{Bias}} \qquad (3.1)$$

Table 1: Aspect Ratio of MOS Transistors for CMOS OTA

MOS Transistor	Width (µm)	Length (µm)
M1,M2	8.24	0.36
M3,,M6	7.2	0.36
M4,M5	14.4	0.36
M9,M12	12.5	0.5
M10, M11	12.5	0.5
M7,M8	7.2	0.36

Table 2: Comparison of Different Techniques with Proposed Technique for realization Low Power Amplifier

Ref.No	Employed Technology	Presented Techniques	No of transistors	Transconductance values	Supply Voltage (V)	Linearity Operation
2	65 nm	PSEUDO OTA	12	0.050 mS	1.2 V	± 0.01 V
3	65 nm	DCRT	21	0.023 mS	1.2 V	± 0.16 V
Proposed Work	65 nm	Feed forward Cascode and DCRT	10	61.8 µA / V - 96.8 µA / V	± 0.7V	± 0.01 V

Table 3: Simulated Parameters of Proposed CMOS OTAs based Low Power Amplifier at Different Bias Currents: I_{Bias} = 1µA - 10 µA .

S.No	Specifications	Simulated
1	CMOS Technology	65 nm
2	Transconductances (µS)	61.8 µA / V - 96.8 µA / V at Different Bias Current 2 µA - 10 µA
3	Bias current (µA)	2 µA - 10 µA
4	% Total Harmonic Distortion	2.83 %
5	Power dissipation (mW)	1.6 mW – 3.89 mW
6	Maximum Input noise (nV)	5.036 nV/$\sqrt{Hz}$

7	Maximum output noise (nV)	28.57 nV / $\sqrt{Hz}$
8	Power Supply Voltage (V)	V_{DD} = - V_{SS} ± 0.70 V
9	Bias Voltage (V)	± 0.50 V
10	Phase Margin	50 deg
11	Offset Voltage (mV)	5 mV
12	Slew Rate (V / µs)	64.33 V/ µs - 77 V/ µs
13	DC Gain (dB)	98 dB
14	Common Mode Rejection Ratio	65 – 90 dB
15	Unity Gain Band Width (KHz)	10.89 KHz
16	Power Consumption	0.86 mW – 0.98 mW
17	Figure of Merit	1.58 – 4.36

V. CMOS Simulation Results

a) Simulated Transconductance for Proposed CMOS OTA

This simulation result presents the transconductance characteristic for proposed CMOS OTA based configuration at 65nm CMOS Technology is presented for obtaining curve between the current flowing from output resistance verses input voltage swing from ± 0.7 - 1.0 V . The supply voltages are taken as VDD = - VSS = ± 0.7V for I_{B1}= 2µA, I_{B2}=5 µA, I_{B3} = 10 µA .The characteristic curve for transconductance is presented with connecting the resistance 75Ω - 100Ω at the output as shown in figure.5.

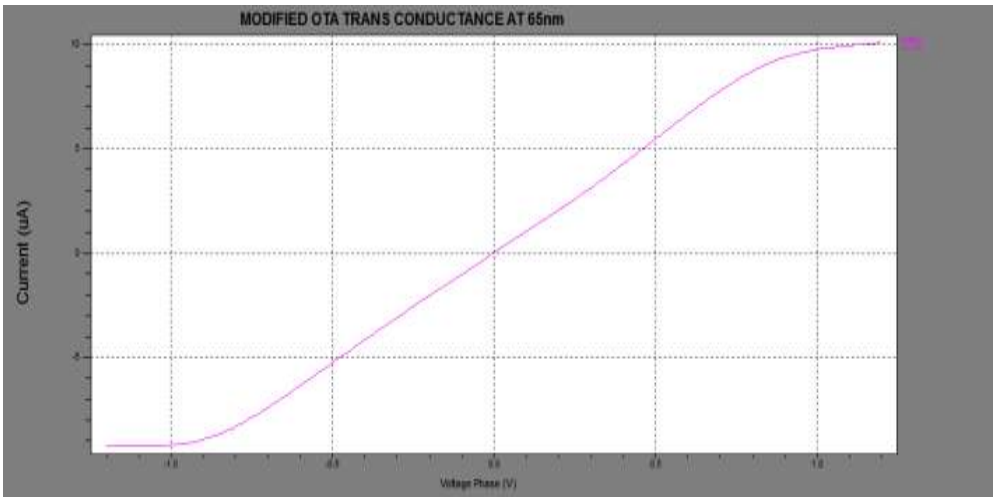

Figure 5. CMOS Simulated Transconductance (Gm) for the proposed OTA Configuration.

b) DC Sweep Response

This simulation result is carried out for the proposed OTA circuit at 65 nm CMOS technology yields the DC .

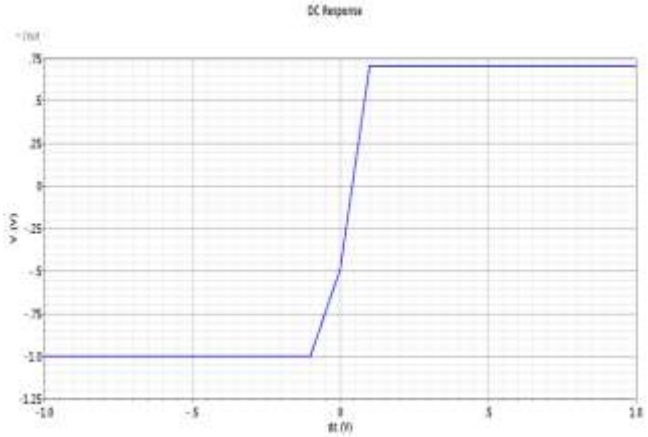

Figure 6. DC Sweep Response for CMOS Differential pair OTA sweep response between the output voltage and DC bias voltage.

The DC response curve of the low power amplifier is presented in figure 6.

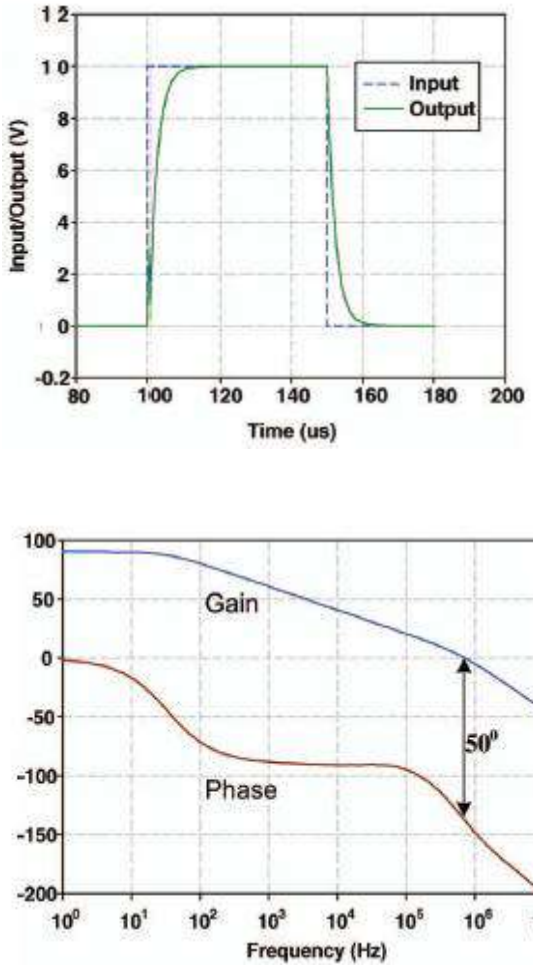

Figure 7. Transient response of the proposed CMOS OTAs based Low Power Amplifier

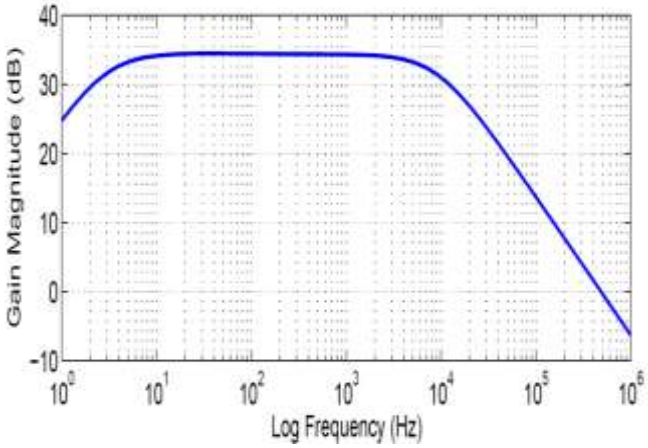

Figure 9. Gain Magnitude response of the proposed CMOS OTAs Based Low Power Amplifier

Figure 8. Frequency and phase response of the proposed CMOS OTAs based Low Power Amplifier

c) CMOS Simulation and Performance Analysis of the proposed CMOS OTAs Based Low Power Amplifier

The proposed configuration is simulated through SPICE simulation using 65 nm TSMC CMOS technology. The proposed CMOS OTAs based low power amplifier is presented three popular techniques are (i) CMOS OTAs based basic differential input single output using feed forward cascode techniques (ii) CMOS OTA based cascode configuration present an active positive feedback with feed forward technique (iii) OTA based cascode feed forward technique with negative feedback for realizing low power amplifier. The CMOS OTAs implementation is presents the performance of the proposed low power amplifier .The power supply and bias voltages are given by $V_{DD} = V_{SS} = \pm 0.7$ V and $V_{Bias} = \pm 0.5$ V. The aspect ratio of the MOS transistors are presented in table 1, The CMOS simulation result yields the value of the transconductance (gm) = 61.8µA/V – 96.8 µA/V at the $V_{DD} = V_{SS} = \pm 0.7$ V and $V_{Bias} = \pm 0.5$ V for CMOS OTA. The transconductance (gm) of OTAs are controlled by the bias currents I_{B1}= 2µA, I_{B2}=5 µA, I_{B3} = 10 µA. The transient response of the proposed CMOS OTAs based Low Power Amplifier is presented in figure 7.

The phase response of the proposed CMOS OTAs based Low Power Amplifier is shown in figure 8. The simulated gain of the proposed CMOS OTAs based Low Power Amplifier at different bias 98dB at the frequency range 10 Hz - 10.89 KHz and phase response of the proposed CMOS OTAs based Low Power Amplifier is 50 deg. The gain magnitude of the proposed CMOS OTAs based Low Power Amplifier is shown in figure 9. The simulated gain magnitude of the proposed CMOS OTAs based Low Power Amplifier is 33- 35 dB at the frequency range 10 Hz - 10.89 KHz and bias currents I_{B1}= 2µA, I_{B2}=5 µA, I_{B3} = 10 µA. The power consumption of the proposed CMOS OTAs based Low Power Amplifier is 0.86 mW – 0.98 mW at the VDD = VSS = ± 0.7 V and $V_{Bias} = \pm 0.5$ V. The total harmonic distortion of the proposed CMOS OTAs based Low Power Amplifier is 2.83% and the power dissipation is1.83 mW – 3.89mW. The input and output noise of the proposed CMOS OTAs based Low Power Amplifier are 5.036 nV / √Hz and 28.57 V / √Hz . Common Mode Rejection of the CMOS OTA is 65 dB – 90 dB and the Slew Rate of the proposed CMOS OTAs for Low Power Amplifier is 64.33 V/ µS – 77 V/ µS. The figure of merits of the proposed CMOS OTAs based low power amplifier has been evaluated 1.58 –4.36.

VI. Performance Evaluation

The performance of the proposed CMOS OTAs low power amplifier is taken from TMSC 65 nm CMOS technology parameters. Low power amplifier in analog electronics enables novel futures in modern biomedical devices and speech processing. It also plays major role for the measuring Frequency and phase response of the proposed CMOS OTAs based Low Power Amplifier in the field of the Engineering and physics such as X ray spectroscopy. The proposed CMOS OTAs based low power amplifier is presented three popular techniques are

(i) CMOS OTAs based basic differential input single output using feed forward cascode techniques. (ii) CMOS OTA based cascode configuration present an active positive feedback with feed forward technique.
(iii) OTA based cascode feed forward technique with negative feedback for realizing low power amplifier. OTA based cascode feed forward technique with negative feedback presents more efficient for CMOS OTA based low power amplifier realized.

VII. Conclusion:

The simulation result presents third technique is more efficient to verified the workability and functionability of the CMOS OTAs low power amplifier is taken from TMSC 65 nm CMOS technology parameters.
OTA based cascode feed forward technique with negative feedback is capable in low voltage design which provides high output impedance to presents high output gain and low power consumption 0.86 mW–0.98mW, LWe increase the gain of the proposed OTA based low power amplifier is implemented in 65 nm CMOS, shows a DC gain of 98 dB, GWB product of 10.89 kHz. The gain boosted current mirroring and self-cascading techniques are used effectively for calculating A low-voltage, micro-power, low-noise, high-gain, high-output swing OTA. OTA based cascode feed forward technique with negative feedback for realizing low power amplifier has some advantageous features:

1) The proposed CMOS OTAs based cascode feed forward technique with negative feedback yields high impedance at the input and output.
2) The proposed CMOS OTAs based cascode feed forward technique with negative feedback based low power amplifier exhibits high stability, high gain , larger band width, high slew rate , improve input / output noise , improve common mode rejection ratio and reduced power supply voltage.
3) The natural frequency (ω_0) of the reported CMOS OTAs based low power amplifier Bandwidth can be controlled with the help of transconductance.
4) The proposed CMOS OTAs based cascode feed forward technique with negative feedback for realization low power amplifier are open area in future research using modern mixed analog signal processing based integrated circuits for achieving high linearity and stability , larger band width and high gain at low voltage.
5) The CMOS OTAs based cascode feed forward technique with negative feedback is used particularly for realization low power amplifiers, modulator and amplitude modulation.
6) The proposed CMOS OTAs based cascode feed forward technique with negative feedback yields high impedance at the input and output.
7) The proposed first two configurations raises the problems in level of integration, low gain, and lower band width and increase power supply voltage and gate level delay.
8) Fully integrated with monolithic ICs,
9) Electronic tunability yields for different pole frequencies at different bias currents.
10) The natural frequency (ω_0) of the reported CMOS OTAs based low power amplifier can be tuned with g_{m2} or gm_2 at constant bandwidth.

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